

PREVIOUS YEAR QUESTION PAPER
CS 405
COMPUTER SYSTEM ARCHITECTURE
MODULE 3 AND 4

DECEMBER 2018

1.a) Draw the state transition graph for a cache block using Goodman's write-once protocol for cache coherence.

b) Design an 8 input omega network using 2X2 switches as building blocks. Show the switch settings for the permutation $\pi_1 = (0,6,4,7,3)(1,5)(2)$. Show the conflicts in switch settings, if any. Explain blocking and non-blocking networks in this context.

2.a) Differentiate between synchronous and asynchronous model of linear pipeline processors.

b) Consider the following pipeline reservation table:

	1	2	3	4
S1	X			X
S2		X		
S3			X	

- i) What are the forbidden latencies?
- ii) Draw the transition diagram.
- iii) List all the simple cycles and greedy cycles.
- iv) Determine the optimal constant latency cycle and minimal average latency (MAL)
- v) Let the pipeline clock period be $\tau = 20\text{ns}$. Determine the throughput of the pipeline.

3.a) Explain full-map directory based protocol.

b) What do you mean by dimension order routing? Consider a 16 node hypercube network. Based on E-cube routing algorithm, show how to route a message from 0010 to 1001. Find all intermediate nodes on routing path.

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David H. Stam



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Table of Contents Computer System Architecture Exam Papers

1. Understanding the eBook Computer System Architecture Exam Papers
 - The Rise of Digital Reading Computer System Architecture Exam Papers
 - Advantages of eBooks Over Traditional Books
2. Identifying Computer System Architecture Exam Papers
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Computer System Architecture Exam Papers
 - User-Friendly Interface
4. Exploring eBook Recommendations from Computer System Architecture Exam Papers
 - Personalized Recommendations
 - Computer System Architecture Exam Papers User Reviews and Ratings
 - Computer System Architecture Exam Papers and Bestseller Lists

5. Accessing Computer System Architecture Exam Papers Free and Paid eBooks
 - Computer System Architecture Exam Papers Public Domain eBooks
 - Computer System Architecture Exam Papers eBook Subscription Services
 - Computer System Architecture Exam Papers Budget-Friendly Options
6. Navigating Computer System Architecture Exam Papers eBook Formats
 - ePub, PDF, MOBI, and More
 - Computer System Architecture Exam Papers Compatibility with Devices
 - Computer System Architecture Exam Papers Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Computer System Architecture Exam Papers
 - Highlighting and Note-Taking Computer System Architecture Exam Papers
 - Interactive Elements Computer System Architecture Exam Papers
8. Staying Engaged with Computer System Architecture Exam Papers
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Computer System Architecture Exam Papers
9. Balancing eBooks and Physical Books Computer System Architecture Exam Papers
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Computer System Architecture Exam Papers
10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
11. Cultivating a Reading Routine Computer System Architecture Exam Papers
 - Setting Reading Goals Computer System Architecture Exam Papers
 - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Computer System Architecture Exam Papers
 - Fact-Checking eBook Content of Computer System Architecture Exam Papers
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning

- Utilizing eBooks for Skill Development
- Exploring Educational eBooks

14. Embracing eBook Trends

- Integration of Multimedia Elements
- Interactive and Gamified eBooks

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