

- DSP slices
 - 18 x 25 signed multiply
 - 48-bit adder/accumulator
- Programmable I/O Blocks
 - Support for common I/O standards including LVCMOS, LVDS, and SSTL
 - 1.2V to 3.3V I/O
 - Built-in programmable I/O delay
- Low-power serial transceivers in selected Zynq-7000 All Programmable SoCs
- An integrated Endpoint/Root port (can be Root Complex when connected to the PS) block for PCI Express in selected Zynq-7000 All Programmable SoCs
- Two 12-bit analog to digital converters (XADC)
 - On-chip voltage and temperature
 - Up to 17 external differential input channels
- PL configuration module

CLBs, Slices, and LUTs

Some key features of the CLB architecture include:

- True 6-input LUTs
- Memory capability within the LUT
- Register and shift register functionality

The LUTs in the Zynq-7000 All Programmable SoC can be configured as either one 6-input LUT (64-bit ROMs) with one output, or as two 5-input LUTs (32-bit ROMs) with separate outputs but common addresses or logic inputs. Each LUT output can optionally be registered in a flip-flop. Four such LUTs and their eight flip-flops as well as multiplexers and arithmetic carry logic form a slice, and two slices form a configurable logic block (CLB). Four of the eight flip-flops per slice (one flip-flop per LUT) can optionally be configured as latches.

Between 25–50% of all slices can also use their LUTs as distributed 64-bit RAM or as 32-bit shift registers (SRL32) or as two SRL16s. Modern synthesis tools take advantage of these highly efficient logic, arithmetic, and memory features.

Clock Management

Some of the key highlights of the clock management architecture include:

- High-speed buffers and routing for low-skew clock distribution
- Frequency synthesis and phase shifting
- Low-jitter clock generation and jitter filtering

Zynq-7000 All Programmable SoCs have up to 8 clock management tiles (CMTs), each consisting of one mixed-mode clock manager (MMCM) and one phase-locked loop (PLL). [Table 5](#) shows the MMCMs for each Zynq device.

Table 5: MMCM Count per Device

Zynq Device	MMCM	PLL
XC7Z010	2	2
XC7Z015	3	3
XC7Z020	4	4
XC7Z030	5	5
XC7Z045	8	8
XC7Z100	8	8

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