$$C_{GSO} = C_{GDO} = C_{cs} \cdot L_D = 1.73 \times 10^{-7} \times 0.2 \times 10^{-4}$$

= $3.46 \times 10^{-12} [F/cm] = 3.46 \times 10^{-10} [F/m]$

Thus, the SPICE input file is as follows:

#1 6 12 4 7 MM1 W-5U L-3U LD=0.2U AS=36P PS=24.4U AD=53P * PD=42.4U .MODEL MM1 NMCS (VTO=0.85 FD=45U LANGUA=0.05 GAMBOA=0.32 * PML=0.615 PS=-0.837 CJ=1.41E-4 CJSW=2.2E-10 * CGSO=3.46E-10 CGDO=3.44E-10 MT=0.33 MTSW=0.5)

4.2 A layout of nMOS transistors in NAND2 gate is shown below. Write a SPICE description corresponding to the layout. The diffusion region between two polysilicon gates can be split equally between the two transistors.

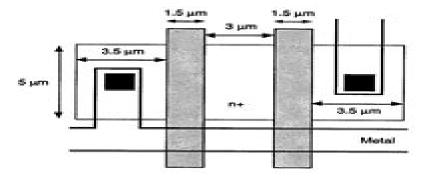


Figure P4.2

SOLUTION:

The SPICE input list could be as follows: ML 2 1 0 0 8800 W-50 L-1.50 As-17.59 Ab-7.59 99-170 90-80 M2 4 3 2 0 8800 W-50 L-1.50 As-7.59 Ab-17.59 99-80 90-170

4.3 Using the SPICE LEVEL I MOSFET model equations, derive an expression for the sensitivity of the drain current I_D with respect to temperature. Calculate the sensitivity at room temperature T=300K by using the values in Example 4.1. For simplicity, assume that n_i is independent of temperature. Also verify your solution numerically by calculating I_D at 310K and then ΔI_A/ΔT.

SOLUTION:

The sensitivity of drain current with respect to temperature T can be expressed by:

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