```
library ieee;
use ieee.std logic 1164.all;
entity decoder 3x8 is
port (a : in std logic vector(0 to 2);
       d : out std logic vector (0 to 7));
end decoder 3x8;
architecture decoder arch of decoder 3x8 is
 begin
  process (a)
   begin
      case a is
          when "000" \Rightarrow d \Leftarrow "00000001";
          when "001" \Rightarrow d \Leftarrow "00000010";
          when "010" \Rightarrow d \Leftarrow "00000100";
          when "011" \Rightarrow d \Leftarrow "00001000";
          when "100" \Rightarrow d \Leftarrow "00010000";
          when "101" => d <= "001000000";
          when "110" \Rightarrow d \Leftarrow "01000000";
          when "111" => d <= "10000000";
          when others => d<= "00000000";
   end case;
  end process;
end decoder arch;
```

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Data corruption during the transmission and reception of data because of noisy channel medium is the most common problem faced in digital communication system Thus it is hard to get the reliable communication Thus to get the error free communication we need Error correction code BCH codes is an acronym for Bose Ray Chaudhuri Hocquenghem invented in 1960s and today they are used as a baseline for many recent Error Correcting Codes BCH codes are powerful class of multiple error correction codes with well defined mathematical properties BCH code is used to correct multiple random error patterns The mathematical properties within which BCH codes are defined are the Galois Field or Finite Field Theory The main focus of this project is to design encoder and decoder architecture for BCH codes. The design of an encoder is based on Liner Feed Back Shift Register used for polynomial division and the decoder design is based on ibm algorithm to correct the errors occurred during transmission Also this project report contains comparison of BCH codes with other Error Correcting codes and gives the detailed explanation of salient feature of BCH codes The combination of BCH codes and LDPC codes are used for error correction for satellite communication standards The BCH codes architecture is described using hardware description language called Verilog and synthesized using Xilinx Webpack 10 1 ISE The performance of the whole model is check in terms of simulation using Xilinx Modelsim **Index to IEEE Publications** Institute of Electrical and Electronics The 11th IEEE International Symposium on Personal, Indoor and Mobile Radio Communications ,2000 Engineers, 1994 Proceedings of the ASP-DAC ... Asia and South Pacific Design Automation Conference, 1995 **Government Reports** Announcements & Index ,1989-05 A VHDL Code Generator for Reed-Solomon Encoders and Decoders Vladimir Glavac,2003

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