

$$C_{GSO} = C_{GDO} = C_{ox} \cdot L_D = 1.73 \times 10^{-7} \times 0.2 \times 10^{-4} \\ = 3.46 \times 10^{-12} [F/cm] = 3.46 \times 10^{-12} [F/m]$$

Thus, the SPICE input file is as follows:

```

M1 6 12 4 7 NMOS W=5U L=30U LD=0.20 AS=34P PS=24.4U AD=93P
+ PD=42.4U
.MODEL NMOS NMOS (VTO=0.85 KP=45U LAMDA=0.05 GAMMA=0.32
+ PHI=0.615 PB=0.837 CJS=1.41E-4 CJSW=3.2E-10
+ CGSO=3.46E-10 CGDO=3.46E-10 NS=0.33 NDSW=0.5)

```

- 4.2 A layout of nMOS transistors in NAND2 gate is shown below. Write a SPICE description corresponding to the layout. The diffusion region between two polysilicon gates can be split equally between the two transistors.

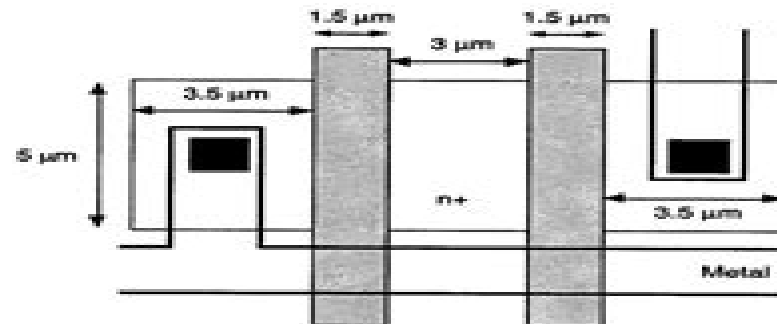


Figure P4.2

**SOLUTION:**

The SPICE input list could be as follows:

```

M1 2 1 0 0 NMOS W=5U L=1.5U AS=17.5P AD=7.5P PS=17U PD=8U
M2 4 3 2 0 NMOS W=5U L=1.5U AS=7.5P AD=17.5P PS=8U PD=17U

```

- 4.3 Using the SPICE LEVEL 1 MOSFET model equations, derive an expression for the sensitivity of the drain current  $I_D$  with respect to temperature. Calculate the sensitivity at room temperature  $T=300K$  by using the values in Example 4.1. For simplicity, assume that  $n_i$  is independent of temperature. Also verify your solution numerically by calculating  $I_D$  at 310K and then  $\Delta I_D / \Delta T$ .

**SOLUTION:**

The sensitivity of drain current with respect to temperature  $T$  can be expressed by:

# Digital Integrated Circuits Solution Manual Martin

**David Baud**



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## **Table of Contents Digital Integrated Circuits Solution Manual Martin**

1. Understanding the eBook Digital Integrated Circuits Solution Manual Martin
  - The Rise of Digital Reading Digital Integrated Circuits Solution Manual Martin
  - Advantages of eBooks Over Traditional Books
2. Identifying Digital Integrated Circuits Solution Manual Martin
  - Exploring Different Genres
  - Considering Fiction vs. Non-Fiction
  - Determining Your Reading Goals
3. Choosing the Right eBook Platform
  - Popular eBook Platforms
  - Features to Look for in an Digital Integrated Circuits Solution Manual Martin
  - User-Friendly Interface
4. Exploring eBook Recommendations from Digital Integrated Circuits Solution Manual Martin
  - Personalized Recommendations
  - Digital Integrated Circuits Solution Manual Martin User Reviews and Ratings
  - Digital Integrated Circuits Solution Manual Martin and Bestseller Lists
5. Accessing Digital Integrated Circuits Solution Manual Martin Free and Paid eBooks
  - Digital Integrated Circuits Solution Manual Martin Public Domain eBooks
  - Digital Integrated Circuits Solution Manual Martin eBook Subscription Services
  - Digital Integrated Circuits Solution Manual Martin Budget-Friendly Options
6. Navigating Digital Integrated Circuits Solution Manual Martin eBook Formats

- ePub, PDF, MOBI, and More
- Digital Integrated Circuits Solution Manual Martin Compatibility with Devices
- Digital Integrated Circuits Solution Manual Martin Enhanced eBook Features
- 7. Enhancing Your Reading Experience
  - Adjustable Fonts and Text Sizes of Digital Integrated Circuits Solution Manual Martin
  - Highlighting and Note-Taking Digital Integrated Circuits Solution Manual Martin
  - Interactive Elements Digital Integrated Circuits Solution Manual Martin
- 8. Staying Engaged with Digital Integrated Circuits Solution Manual Martin
  - Joining Online Reading Communities
  - Participating in Virtual Book Clubs
  - Following Authors and Publishers Digital Integrated Circuits Solution Manual Martin
- 9. Balancing eBooks and Physical Books Digital Integrated Circuits Solution Manual Martin
  - Benefits of a Digital Library
  - Creating a Diverse Reading Collection Digital Integrated Circuits Solution Manual Martin
- 10. Overcoming Reading Challenges
  - Dealing with Digital Eye Strain
  - Minimizing Distractions
  - Managing Screen Time
- 11. Cultivating a Reading Routine Digital Integrated Circuits Solution Manual Martin
  - Setting Reading Goals Digital Integrated Circuits Solution Manual Martin
  - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Digital Integrated Circuits Solution Manual Martin
  - Fact-Checking eBook Content of Digital Integrated Circuits Solution Manual Martin
  - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
  - Utilizing eBooks for Skill Development
  - Exploring Educational eBooks
- 14. Embracing eBook Trends
  - Integration of Multimedia Elements
  - Interactive and Gamified eBooks

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