

ENCOUNTER CONFORMAL ECO DESIGNER

Cadence® Encounter® Conformal® ECO Designer enables designers to implement RTL engineering change orders (ECOs) for pre- and post-mask layout. It combines automatic ECO analysis and design netlist modification with world-class equivalence checking to provide superior performance, productivity, capacity, and ease-of-use.

ENCOUNTER CONFORMAL TECHNOLOGY

To shorten overall design-cycle times and minimize silicon re-spins, designers need production-proven validation. Encounter Conformal verification technologies offer the most comprehensive solutions for equivalence checking, design constraint management, functional ECO analysis and generation, and low-power design verification.

ENGINEERING CHANGE ORDERS

Engineering change orders (ECOs) have a wide variety of implementations that range from adding or removing logic to a design to more subtle changes such as cleaning up routing for signal integrity. A logical change to a design netlist is referred to as functional ECO while all other changes are classified as non-functional. All ECOs are focused on delivering products to market as fast as possible with minimal risk to correctness and schedule. Engineering and

management recognize ECOs as a time of high stress, long work hours, and uncertainty. Even if the logic change is implemented in the netlist, there might not be enough spare gates on the mask to implement the change.

A better method is needed for implementing ECOs. Available flows for processing ECOs may remove some of the uncertainty of whether the product will work, but they are still a manual process that typically requires many cycles to achieve correct implementation. And once the ECO is logically implemented in the netlist, there is no guarantee if the change can be implemented in the physical netlist. If the ECO were implemented with only metal-layer changes, the cost would be greatly reduced. Having this early knowledge of implementability, a design team can change plans and target workable solutions rather than wasting time in failed attempts and extended schedules.

ENCOUNTER CONFORMAL ECO DESIGNER

Cadence offers a complete ECO solution that spans different parts of the RTL-to-GDS flow to achieve the highest quality ECOs. This solution consists of Encounter Conformal ECO Designer coupled with the Cadence SoC Encounter™ RTL-to-GDS2 System. This combined solution brings automation and predictability to the ECO process.

Encounter Conformal ECO Designer is a unique technology that offers functional ECO analysis, optimization, and generation capability. It combines proven equivalence checking and functional checks, and uses formal techniques to analyze and implement the functional ECO. Encounter Conformal ECO Designer is available in two configurations: an XL package, which targets primarily the pre-mask ECO flow; and a GX package, which additionally targets the post-mask ECO flow using metal-only layers and spare gates.

Cadence Encounter User Manual

John Curwen



Cadence Encounter User Manual:

Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits Sandeep K. Goel, Krishnendu Chakrabarty, 2017-12-19 Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits ICs. However, the increased complexity and nanometer size features of modern ICs make them susceptible to manufacturing defects as well as performance and quality issues. Testing for Small Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations, power supply noise, crosstalk, resistive opens, bridges, and design for manufacturing DfM related rule violations. The book also addresses testing for small delay defects SDDs which can cause immediate timing failures on both critical and non-critical paths in the circuit. Overviews semiconductor industry test challenges and the need for SDD testing including basic concepts and introductory material. Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics. Reviews SDD testing based on alternative methods that explore new metrics, top off ATPG and circuit topology based solutions. Highlights the advantages and disadvantages of a diverse set of metrics and identifies scope for improvement. Written from the triple viewpoint of university researchers, EDA tool developers, and chip designers and tool users, this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective. The book is designed as a one-stop reference for current industrial practices, research challenges in the domain of SDD testing, and recent developments in SDD solutions.

Nanometer Technology Designs Nisar Ahmed, 2010-02-26 Adopting new fabrication technologies not only provides higher integration and enhances performance but also increases the types of manufacturing defects. With design size in millions of gates and working frequency in GHz, timing-related defects have become a high proportion of the total chip defects. For nanometer technology designs, the stuck-at-fault test alone cannot ensure a high quality level of chips. At-speed tests using the transition fault model have become a requirement in technologies below 180nm. Traditional at-speed test methods cannot guarantee high quality test results as they face many new challenges. Supply noise including IR drop, ground bounce, and Ldi dt effects on chip performance, high test pattern volume, low fault defect coverage, small delay defect test pattern generation, high cost of test implementation and application, and utilizing low cost testers are among these challenges. This book discusses these challenges in detail and proposes new techniques and methodologies to improve the overall quality of the transition fault test.

Test and Diagnosis for Small-Delay Defects Mohammad Tehranipoor, Ke Peng, Krishnendu Chakrabarty, 2011-09-08 This book will introduce new techniques for detecting and diagnosing small delay defects in integrated circuits. Although this sort of timing defect is commonly found in integrated circuits manufactured with nanometer technology, this will be the first book to introduce effective and scalable methodologies for screening and diagnosing small delay defects including important parameters such as process variations, crosstalk, and power supply noise.

Design and Process Integration for Microelectronic Manufacturing, 2005

Synthesis Methodology for Built-in At-speed

Testing Yinghua Li, 2005 **FPGA ...**, 2006 **The teacher's manual of the tonic sol-fa method** John Curwen, 1902
Electronic Design, 2007 *EDN*, 2008 *Journal of the United States Infantry Association*, 1950 **Instructions to
 Young Fencers** Gillan Sheen, 1958 **Indiana Farmer's Guide**, 1921 **A Low Power Design Methodology with
 Multi-VDD and Voltage Islands** Huaizhi Wu, 2007 *Oceanic Music Encounters* Mervyn McLean, 2007

Mervyn Evan McLean teacher mentor researcher and archivist is the worthy recipient of this set of essays *Oceanic Music Encounters* the Print Resource and the Human Resource The authors include colleagues and former students of an academic who was a practising ethnomusicologist only three years after the term was coined Although most of his university career was spent at the University of Auckland Mervyn's influence in the fields of Pacific music research and archiving were such that the contributions in this volume are the result of both distant reputation and personal acquaintance The volume is the product of the Study Group on Musics of Oceania within the International Council for Traditional Music of which Mervyn has been a member for many years The volume title is intended to encompass the span of Mervyn's professional interests which include the role of archives in Oceanic music research and performance material culture collections in music research and performance the role of transcription in music research and performance the importance of bibliographic research in tracing the connections between the past and the present the significance of collaboration in research particularly with scholars in other disciplines and its significance to performance and the colonial encounter and its implications for historical and contemporary performance *Design and Process Integration for Microelectronic Manufacturing II* [sic] Lars W. Liebmann, 2004

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