Memory Hierarchy Design

Cache And Memory Hierarchy Design A Performance Directed Approach Hardback

International Business Machines Corporation. Research Division,Richard E. Matick

Cache And Memory Hierarchy Design A Performance Directed Approach Hardback:

Cache and Memory Hierarchy Design Steven A. Przybylski,1990 A widely read and authoritative book for hardware and software designers This innovative book exposes the characteristics of performance optimal single and multi level cache hierarchies by approaching the cache design process through the novel perspective of minimizing execution time

Performance-directed Memory Hierarchy Design Steven A. Przybylski,Stanford University. Computer Systems Laboratory,1988   *Exploring Memory Hierarchy Design with Emerging Memory Technologies* Guangyu Sun,2013-09-18 This book equips readers with tools for computer architecture of high performance low power and high reliability memory hierarchy in computer systems based on emerging memory technologies such as STTRAM PCM FBDRAM etc The techniques described offer advantages of high density near zero static power and immunity to soft errors which have the potential of overcoming the memory wall The authors discuss memory design from various perspectives emerging memory technologies are employed in the memory hierarchy with novel architecture modification hybrid memory structure is introduced to leverage advantages from multiple memory technologies an analytical model named Moguls is introduced to explore quantitatively the optimization design of a memory hierarchy finally the vulnerability of the CMPs to radiation based soft errors is improved by replacing different levels of on chip memory with STT RAMs   **Redesigning the Memory Hierarchy to Exploit Static and Dynamic Application Information** Po-An Tsai,2019 Memory hierarchies are crucial to performance and energy efficiency but current systems adopt rigid hardware managed cache hierarchies that cause needless data movement The root cause for the inefficiencies of cache hierarchies is that they adopt a legacy interface and ignore most application information Specifically they are structured as a rigid hierarchy of progressively larger and slower cache levels with sizes and policies fixed at design time Caches expose a flat address space to programs that hides the hierarchy s structure and transparently move data across cache levels in fixed size blocks using simple fixed heuristics Besides squandering valuable application level information this design is very costly providing the illusion of a flat address space requires complex address translation machinery such as associative lookups in caches This thesis proposes to redesign the memory hierarchy to better exploit application information We take a cross layer approach that redesigns the hardware software interface to put software in control of the hierarchy and naturally convey application semantics We focus on two main directions First we design reconfigurable cache hierarchies that exploit dynamic application information to optimize their structure on the fly approaching the performance of the best application specific hierarchy Hardware monitors application memory behavior at low overhead and a software runtime uses this information to periodically reconfigure the system This approach enables software to i build single or multi level virtual cache hierarchies tailored to the needs of each application making effective use of spatially distributed and heterogeneous e g SRAM and stacked DRAM cache banks ii replicate shared data near optimally to minimize on chip and off chip traffic and iii schedule computation across systems with

heterogeneous hierarchies e g systems with near data processors Specializing the memory system to each application improves performance and energy efficiency since applications can avoid using resources that they do not benefit from and use the remaining resources to hold their data at minimum latency and energy For example virtual cache hierarchies improve full system energy delay product EDP by up to 85% over a combination of state of the art techniques Second we redesign the memory hierarchy to exploit static application information by managing variable sized objects the natural unit of data access in programs instead of fixed size cache lines We present the Hotpads object based hierarchy which leverages object semantics to hide the memory layout and dispense with the flat address space interface Similarly to how memory safe languages abstract the memory layout Hotpads exposes an interface based on object pointers that disallows arbitrary address arithmetic This avoids the need for associative caches Instead Hotpads moves objects across a hierarchy of directly addressed memories It rewrites pointers to avoid most associative lookups provides hardware support for memory management and unifies hierarchical garbage collection and data placement Hotpads also enables many new optimizations For instance we have designed Zippads a memory hierarchy that leverages Hotpads to compress objects Leveraging object semantics and the ability to rewrite pointers in Hotpads Zippads compresses and stores objects more compactly with a novel compression algorithm that exploits redundancy across objects Though object based languages are often seen as sacrificing performance for productivity this work shows that hardware can exploit this abstraction to improve performance and efficiency over cache hierarchies Hotpads reduces dynamic memory hierarchy energy by 2 6x and improves performance by 34% and Zippads reduces main memory footprint by 2x while improving performance by 30%   *The Cache Memory Book* Jim Handy,1998-01-13 The Second Edition of The Cache Memory Book introduces systems designers to the concepts behind cache design The book teaches the basic cache concepts and more exotic techniques It leads readers through someof the most intricate protocols used in complex multiprocessor caches Written in an accessible informal style this text demystifies cache memory design by translating cache concepts and jargon into practical methodologies and real life examples It also provides adequate detail to serve as a reference book for ongoing work in cache memory design The Second Edition includes an updated and expanded glossary of cache memory terms and buzzwords The book provides new real world applications of cache memory design and a new chapter on cachetricks Illustrates detailed example designs of caches Provides numerous examples in the form of block diagrams timing waveforms state tables and code traces Defines and discusses more than 240 cache specific buzzwords comparing in detail the relative merits of different design methodologies Includes an extensive glossary complete with clear definitions synonyms and references to the appropriate text discussions   <u>A Primer on Compression in the Memory Hierarchy</u> Somayeh Sardashti,Angelos Arelakis,Per Stenström,David A. Wood,2022-05-31 This synthesis lecture presents the current state of the art in applying low latency lossless hardware compression algorithms to cache memory and the memory cache link There are many non trivial challenges that must be addressed to make data

compression work well in this context First since compressed data must be decompressed before it can be accessed decompression latency ends up on the critical memory access path This imposes a significant constraint on the choice of compression algorithms Second while conventional memory systems store fixed size entities like data types cache blocks and memory pages these entities will suddenly vary in size in a memory system that employs compression Dealing with variable size entities in a memory system using compression has a significant impact on the way caches are organized and how to manage the resources in main memory We systematically discuss solutions in the open literature to these problems Chapter 2 provides the foundations of data compression by first introducing the fundamental concept of value locality We then introduce a taxonomy of compression algorithms and show how previously proposed algorithms fit within that logical framework Chapter 3 discusses the different ways that cache memory systems can employ compression focusing on the trade offs between latency capacity and complexity of alternative ways to compact compressed cache blocks Chapter 4 discusses issues in applying data compression to main memory and Chapter 5 covers techniques for compressing data on the cache to memory links This book should help a skilled memory system designer understand the fundamental challenges in applying compression to the memory hierarchy and introduce him her to the state of the art techniques in addressing them

Compiler Directed Memory Hierarchy Design and Management in Chip Multiprocessors Ozcan Ozturk,2007 Two trends namely increasing importance of memory subsystems and increasing use of chip multiprocessing motivate conducting research on memory hierarchy optimization for chip multiprocessors One of the critical research topics along this direction is to design an application specific customized software managed on chip memory hierarchy for a chip multiprocessor Another important issue is to optimize the application code and data for such a customized on chip memory hierarchy This thesis proposes solutions to the problem of memory hierarchy design and data access management First an integer linear programming ILP based solution to the combined problem of memory hierarchy design and data allocation in the context of embedded chip multiprocessors is given The proposed solution uses compiler analysis to extract data access patterns of parallel processors and employs integer linear programming for determining the optimal on chip memory partitioning across processors and data allocations across memory components Second we present and evaluate a compiler driven approach to data compression for reducing memory space occupancy Our goal is to study how automated compiler support can help in deciding the set of data elements to compress decompress and the points during execution at which these compressions decompressions should be performed The proposed compiler support achieves this by analyzing the source code of the application to be optimized and identifying the order in which the different data blocks are accessed Based on this analysis the compiler then inserts compression decompression calls in the application code The compression calls target the data blocks that are not expected to be used in the near future whereas the decompression calls target those data blocks with expected reuse but currently in compressed form Third we present a constraint network based formulation of the integrated

loop data optimization problem to improve locality of data accesses for a given application code We present two alternate solutions to the data locality problem with our constraint network based formulation and discuss the pros and cons of each scheme The first solution is a pure backtracking based one whereas the second one improves upon the first one by employing three additional optimizations including backjumping Fourth we extend our constraint network based approach to code parallelization for chip multiprocessors Fifth we explore how processor cores and storage blocks can be placed in a 3D architecture to minimize data access costs under temperature This process topology exploration has been implemented using integer linear programming Finally we present a Scratch Pad Memory space management technique for chip multiprocessors We focus on the management of a scratch pad space shared by multiple applications executing at the same time that can potentially share data The proposed approach has three major components a compiler analysis phase a runtime space partitioner and a local partitioning phase This thesis also presents experimental evidence demonstrating the success of each of the proposed techniques and compares our results with those obtained through previously proposed approaches

Multi-Core Cache Hierarchies Rajeev Balasubramonian,Norman P. Jouppi,Naveen Muralimanohar,2011-06-06 A key determinant of overall system performance and power dissipation is the cache hierarchy since access to off chip memory consumes many more cycles and energy than on chip accesses In addition multi core processors are expected to place ever higher bandwidth demands on the memory system All these issues make it important to avoid off chip memory access by improving the efficiency of the on chip cache Future multi core processors will have many large cache banks connected by a network and shared by many cores Hence many important problems must be solved cache resources must be allocated across many cores data must be placed in cache banks that are near the accessing core and the most important data must be identified for retention Finally difficulties in scaling existing technologies require adapting to and exploiting new technology constraints The book attempts a synthesis of recent cache research that has focused on innovations for multi core processors It is an excellent starting point for early stage graduate students researchers and practitioners who wish to understand the landscape of recent cache research The book is suitable as a reference for advanced computer architecture classes as well as for experienced researchers and VLSI engineers Table of Contents Basic Elements of Large Cache Design Organizing Data in CMP Last Level Caches Policies Impacting Cache Hit Rates Interconnection Networks within Large Caches Technology Concluding Remarks   Analysis of Cache Performance for Operating Systems and Multiprogramming Agarwal,2012-12-06 As we continue to build faster and fast er computers their performance is be coming increasingly dependent on the memory hierarchy Both the clock speed of the machine and its throughput per clock depend heavily on the memory hierarchy The time to complet e a cache acce88 is oft en the factor that det er mines the cycle time The effectiveness of the hierarchy in keeping the average cost of a reference down has a major impact on how close the sustained per formance is to the peak performance Small changes in the performance of the memory hierarchy cause large changes in overall system performance

The strong growth of ruse machines whose performance is more tightly coupled to the memory hierarchy has created increasing demand for high performance memory systems This trend is likely to accelerate the improvements in main memory performance will be small compared to the improvements in processor performance This difference will lead to an increasing gap between prOCe880r cycle time and main memory acce time This gap must be closed by improving the memory hierarchy Computer architects have attacked this gap by designing machines with cache sizes an order of magnitude larger than those appearing five years ago Microproce880r based RISe systems now have caches that rival the size of those in mainframes and supercomputers   The Fractal Structure of Data Reference Bruce McNutt,2005-11-24 The architectural concept of a memory hierarchy has been immensely successful making possible today s spectacular pace of technology evolution in both the volume of data and the speed of data access Its success is difficult to understand however when examined within the traditional memoryless framework of performance analysis The memoryless framework cannot properly reflect a memory hierarchy s ability to take advantage of patterns of data use that are transient The Fractal Structure of Data Reference Applications to the Memory Hierarchy both introduces and justifies empirically an alternative modeling framework in which arrivals are driven by a statistically self similar underlying process and are transient in nature The substance of this book comes from the ability of the model to impose a mathematically tractable structure on important problems involving the operation and performance of a memory hierarchy It describes events as they play out at a wide range of time scales from the operation of file buffers and storage control cache to a statistical view of entire disk storage applications Striking insights are obtained about how memory hierarchies work and how to exploit them to best advantage The emphasis is on the practical application of such results The Fractal Structure of Data Reference Applications to the Memory Hierarchy will be of interest to professionals working in the area of applied computer performance and capacity planning particularly those with a focus on disk storage The book is also an excellent reference for those interested in database and data structure research
    Memory Systems Bruce Jacob,David Wang,Spencer Ng,2010-07-28 Is your memory hierarchy stopping your microprocessor from performing at the high level it should be Memory Systems Cache DRAM Disk shows you how to resolve this problem The book tells you everything you need to know about the logical design and operation physical design and operation performance characteristics and resulting design trade offs and the energy consumption of modern memory hierarchies You learn how to to tackle the challenging optimization problems that result from the side effects that can appear at any point in the entire hierarchy As a result you will be able to design and emulate the entire memory hierarchy Understand all levels of the system hierarchy Xcache DRAM and disk Evaluate the system level effects of all design choices Model performance and energy consumption for each component in the memory hierarchy   **High Performance Memory Systems** Haldun Hadimioglu,David Kaeli,Jeffrey Kuskin,Ashwini Nanda,Josep Torrellas,2011-06-27 The State of Memory Technology Over the past decade there has been rapid growth in the speed of micropro cessors CPU speeds are

approximately doubling every eighteen months while main memory speed doubles about every ten years The International Tech nology Roadmap for Semiconductors ITRS study suggests that memory will remain on its current growth path The ITRS short and long term targets indicate continued scaling improvements at about the current rate by 2016 This translates to bit densities increasing at two times every two years until the introduction of 8 gigabit dynamic random access memory DRAM chips after which densities will increase four times every five years A similar growth pattern is forecast for other high density chip areas and high performance logic e g microprocessors and application specific inte grated circuits ASICs In the future molecular devices 64 gigabit DRAMs and 28 GHz clock signals are targeted Although densities continue to grow we still do not see significant advances that will improve memory speed These trends have created a problem that has been labeled the Memory Wall or Memory Gap   *Problems, Directions and Issues in Memory Hierarchies* Alan Jay Smith,1984 The effective and efficient use of the memory hierarchy of the computer system is one of the if not the single most important aspect of computer system design and use Cache memory performance is often the limiting factor in CPU performance and cache memories also serve to cut the memory traffic in multiprocessor systems Multiprocessor systems are also requiring advances in cache architecture with respect to cache consistency Similarly the study of the best means to share main memory is an important research topic Disk cache is becoming important for performance in high end computer systems and is now widely available commercially there are many related research problems The development of mass storage especially optical disk will promote research in effective algorithms for file management and migration In this paper we look at each component of the memory hierarchy and address two issues what are likely directions for development and what are the interesting research problems   *Emerging Memory Technologies* Yuan Xie,2013-10-21 This book explores the design implications of emerging non volatile memory NVM technologies on future computer memory hierarchy architecture designs Since NVM technologies combine the speed of SRAM the density of DRAM and the non volatility of Flash memory they are very attractive as the basis for future universal memories This book provides a holistic perspective on the topic covering modeling design architecture and applications The practical information included in this book will enable designers to exploit emerging memory technologies to improve significantly the performance power reliability of future mainstream integrated circuits

Memory Hierarchies: Analytical Analysis of Finite Cache Penalty with Applications to a Four Level Hierarchy Including SRAM/DRAM Comparisons International Business Machines Corporation. Research Division,Richard E. Matick,1998 Abstract The performance of a memory hierarchy associated with any computing system is becoming the major performance determining factor As technology allows faster processors and larger main memory more levels of caching are required to bridge the access gap between memory and processor In addition moderately fast DRAM s are becoming available which have the potential to replace SRAM s at various levels Even though DRAM will remain somewhat slower than SRAM the potentially 4 to 16 times larger density of DRAM in the same area can often compensate for the slower speed

While an accurate performance evaluation tool requires TRACE driven simulators approximations and significant insight can be obtained with simple performance analysis based on Miss Ratios and some empirical relations between various levels of a memory hierarchy The first part of this work brings together some of these analytical techniques both as a reference and a learning tool for those needing to know more about memory hierarchy performance The second part uses the various analytical approximations to show some interesting behavior of a 4 level memory hierarchy In addition the performance of such a hierarchy using an SRAM L3 is compared for various conditions with that using a DRAM L3 Such approximation give sic valuable insights which can be obtained easily and quickly thus serving as design guidelines but not final performance evaluators   **Multi-tier Data Access and Hierarchical Memory Design** Marwan Sleiman,2007   **Hardware and Compiler-directed Cache Coherence in Large-scale Multiprocessors** Lynn Choi,Pen-Chung Yew,University of Illinois at Urbana-Champaign. Department of Computer Science,1996 Abstract In this paper we study a hardware supported compiler directed HSCD cache coherence scheme which can be implemented on a large scale multiprocessor using off the shelf microprocessors such as the Cray T3D The scheme can be adapted to various cache organizations including multi word cache lines and byte addressable architectures Several system related issues including critical sections inter thread communication and task migration have also been addressed The cost of the required hardware support is minimal and proportional to the cache size The necessary compiler algorithms including intra and interprocedural array data flow analysis have been implemented on the Polaris parallelizing compiler 33 From our simulation study using the Perfect Club benchmarks 5 we found that in spite of the conservative analysis made by the compiler the performance of the proposed HSCD scheme can be comparable to that of a full map hardware directory scheme Given its comparable performance and reduced hardware cost the proposed scheme can be a viable alternative for large scale multiprocessors such as the Cray T3D which rely on users to maintain data coherence   **The Design and Performance Evaluation of Cache Memory Systems** Chinh Gia Pham,1989   **Design and Analysis of a Memory Hierarchy for a Very High Performance Multiprocessor Configuration** Evan Michael Tick,1982   **A Systematic Approach for the Design of an Optimal Performance Cache** Mohammad Wasique,1991

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