# **ENCOUNTER TEST ARCHITECT**

Creating a complete manufacturing test methodology typically requires post-netlist use of disparate software products— a tedious and error-prone process that results in silicon re-designs, high cost, and insufficient product quality and devices that consume too much power during manufacturing test. Cadence\* Encounter\* Test Architect accelerates the development of a higher-quality test infrastructure for hierarchical and flat nanometer designs. With this unified methodology for specifying, inserting, and verifying full-chip tests, design teams can minimize cost of test.

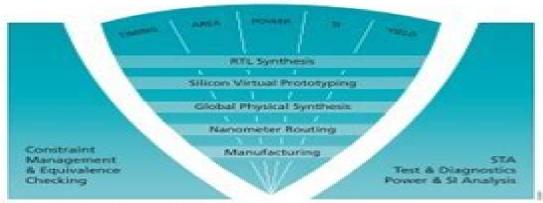
#### **ENCOUNTER TEST**

Encounter Test, a key technology in the Cadence Encounter digital IC design platform, delivers the industry's most advanced test solution from RTL to slicon. It includes three component technologies. Encounter Test Architect, to minimize cost of test. Encounter True-Time Test, to ensure quality of shipped sil-con, and Encounter Diagnostics, to accelerate yield ramp.

#### ENCOUNTER TEST ARCHITECT

Encounter Test Architect is the inclustry's first full-chip test architecture-development product. It supports scan, scalable compression, memory 85T, on-product clock generation, boundary scan, and 900 test. Encounter Test Architect enables a unified specify-insert-verify methodology for design-for-test and test infrastructure including fow low power designs. Using test infrastructure synthesis and the Common Power Format (CPF), it creates, inserts, hierarchically connects, and verifies all of the test structures for a design based on the user's specification. The result is

#### ENCOUNTER



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# **Cadence Encounter Test User Guide**

Jianjun Gao

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Test and Diagnosis for Small-Delay Defects Mohammad Tehranipoor, Ke Peng, Krishnendu Chakrabarty, 2011-09-08 This book will introduce new techniques for detecting and diagnosing small delay defects in integrated circuits Although this sort of timing defect is commonly found in integrated circuits manufactured with nanometer technology this will be the first book to introduce effective and scalable methodologies for screening and diagnosing small delay defects including important parameters such as process variations crosstalk and power supply noise Transaction-Level Power Modeling Amr Baher Darwish, Magdy Ali El-Moursy, Mohamed Amin Dessouky, 2019-08-01 This book describes for readers a methodology for dynamic power estimation using Transaction Level Modeling TLM The methodology exploits the existing tools for RTL simulation design synthesis and SystemC prototyping to provide fast and accurate power estimation using Transaction Level Power Modeling TLPM Readers will benefit from this innovative way of evaluating power on a high level of abstraction at an early stage of the product life cycle decreasing the number of the expensive design iterations Nanometer Technology **Designs** Nisar Ahmed, 2010-02-26 Adopting new fabrication technologies not only provides higher integration and enhances performance but also increases the types of manufacturing defects With design size in millions of gates and working frequency in GHz timing related defects havy become a high proportion of the total chip defects For nanometer technology designs the stuck at fault test alone cannot ensure a high quality level of chips At speed tests using the transition fault model has become a requirement in technologies below 180nm Traditional at speed test methods cannot guarantee high quality test results as they face many new challenges Supply noise including IR drop ground bounce and Ldi dt effects on chip performance high test pattern volume low fault defect coverage small delay defect test pattern generation high cost of test implementation and application and utilizing low cost testers are among these challenges This book discusses these challenges in detail and proposes new techniques and methodologies to improve the overall quality of the transition fault test

Synthesis Methodology for Built-in At-speed Testing Yinghua Li,2005 Power Management in Mobile Devices
Findlay Shearer,2011-04-01 Sealed Lead Acid Nickel Cadmium Lithium Ion How do you balance battery life with
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mobility but demands power longevity in wireless devices As more and more features computing power and memory are
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