$$C_{GSO} = C_{GDO} = C_{cs} \cdot L_D = 1.73 \times 10^{-7} \times 0.2 \times 10^{-4}$$

= $3.46 \times 10^{-12} [F/cm] = 3.46 \times 10^{-10} [F/m]$

Thus, the SPICE input file is as follows:

#1 6 12 4 7 MM1 W-5U L-3U LD=0.2U AS=36P PS=24.4U AD=53P * PD=42.4U .MODEL MM1 NHOS (VTO=0.85 FD=45U LANGUA=0.05 GAMBOA=0.32 * PMI=0.615 PH=0.837 CJ=1.41E=4 CJMM=2.2E=10 * CGSO=3.46E=10 CGDO=3.46E=10 MT=0.33 MTMM=0.5)

4.2 A layout of nMOS transistors in NAND2 gate is shown below. Write a SPICE description corresponding to the layout. The diffusion region between two polysilicon gates can be split equally between the two transistors.

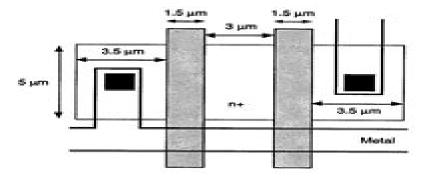


Figure P4.2

SOLUTION:

The SPICE input list could be as follows: ML 2 1 0 0 8800 W-50 L-1.50 As-17.59 Ab-7.59 99-170 90-80 M2 4 3 2 0 8800 W-50 L-1.50 As-7.59 Ab-17.59 99-80 90-170

4.3 Using the SPICE LEVEL I MOSFET model equations, derive an expression for the sensitivity of the drain current I_D with respect to temperature. Calculate the sensitivity at room temperature T=300K by using the values in Example 4.1. For simplicity, assume that n_i is independent of temperature. Also verify your solution numerically by calculating I_D at 310K and then ΔI_A/ΔT.

SOLUTION:

The sensitivity of drain current with respect to temperature T can be expressed by:

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Guillaume Favre

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Table of Contents Digital Integrated Circuits Solution Manual Martin

- 1. Understanding the eBook Digital Integrated Circuits Solution Manual Martin
 - The Rise of Digital Reading Digital Integrated Circuits Solution Manual Martin
 - Advantages of eBooks Over Traditional Books
- 2. Identifying Digital Integrated Circuits Solution Manual Martin
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
- 3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Digital Integrated Circuits Solution Manual Martin
 - User-Friendly Interface
- 4. Exploring eBook Recommendations from Digital Integrated Circuits Solution Manual Martin

- Personalized Recommendations
- Digital Integrated Circuits Solution Manual Martin User Reviews and Ratings
- Digital Integrated Circuits Solution Manual Martin and Bestseller Lists
- 5. Accessing Digital Integrated Circuits Solution Manual Martin Free and Paid eBooks
 - Digital Integrated Circuits Solution Manual Martin Public Domain eBooks
 - Digital Integrated Circuits Solution Manual Martin eBook Subscription Services
 - o Digital Integrated Circuits Solution Manual Martin Budget-Friendly Options
- 6. Navigating Digital Integrated Circuits Solution Manual Martin eBook Formats
 - o ePub, PDF, MOBI, and More
 - o Digital Integrated Circuits Solution Manual Martin Compatibility with Devices
 - Digital Integrated Circuits Solution Manual Martin Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Digital Integrated Circuits Solution Manual Martin
 - Highlighting and Note-Taking Digital Integrated Circuits Solution Manual Martin
 - $\circ\,$ Interactive Elements Digital Integrated Circuits Solution Manual Martin
- 8. Staying Engaged with Digital Integrated Circuits Solution Manual Martin
 - o Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Digital Integrated Circuits Solution Manual Martin
- 9. Balancing eBooks and Physical Books Digital Integrated Circuits Solution Manual Martin
 - $\circ\,$ Benefits of a Digital Library
 - o Creating a Diverse Reading Collection Digital Integrated Circuits Solution Manual Martin
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Digital Integrated Circuits Solution Manual Martin
 - Setting Reading Goals Digital Integrated Circuits Solution Manual Martin
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Digital Integrated Circuits Solution Manual Martin

- Fact-Checking eBook Content of Digital Integrated Circuits Solution Manual Martin
- Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
- 14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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