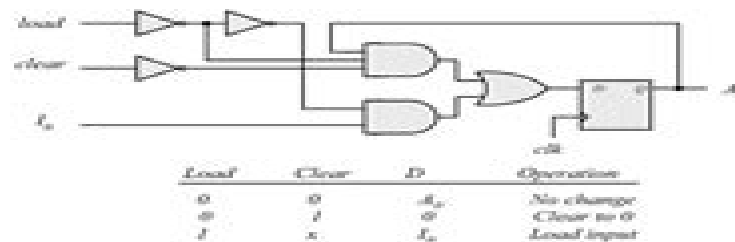


CHAPTER 6

- 6.1** The structure shown below gates the clock through a nand gate. In practice, the circuit can exhibit two problems if the load signal is asynchronous: (1) the gated clock arrives in the setup interval of the clock of the flip-flop, causing metastability, and (2) the load signal truncates the width of the clock pulse. Additionally, the propagation delay through the nand gate might compromise the synchronicity of the overall circuit.



- 6.2** Modify Fig. 6.2, with each stage replicating the first stage shown below:



Note: In this design, *load* has priority over *clear*.

- 6.3** Serial data is transferred one bit at a time. Parallel data is transferred n bits at a time ($n > 1$).
- A shift register can convert serial data into parallel data by first shifting one bit a time into the register and then taking the parallel data from the register outputs.
- A shift register with parallel load can convert parallel data to a serial format by first loading the data in parallel and then shifting the bits one at a time.
- 6.4** $101101 \Rightarrow 1101; 0110; 1011; 1101; 0110; 1011$
- 6.5** (a) See Fig. 11.19: IC 74194
- (b) See Fig. 11.20. Connect two 74194 ICs to form an 8-bit register.

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Lingjun Ying



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Table of Contents Digital Logic And Computer Design Solution Manual

1. Understanding the eBook Digital Logic And Computer Design Solution Manual
 - The Rise of Digital Reading Digital Logic And Computer Design Solution Manual
 - Advantages of eBooks Over Traditional Books
2. Identifying Digital Logic And Computer Design Solution Manual
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Digital Logic And Computer Design Solution Manual
 - User-Friendly Interface
4. Exploring eBook Recommendations from Digital Logic And Computer Design Solution Manual
 - Personalized Recommendations
 - Digital Logic And Computer Design Solution Manual User Reviews and Ratings
 - Digital Logic And Computer Design Solution Manual and Bestseller Lists
5. Accessing Digital Logic And Computer Design Solution Manual Free and Paid eBooks
 - Digital Logic And Computer Design Solution Manual Public Domain eBooks
 - Digital Logic And Computer Design Solution Manual eBook Subscription Services
 - Digital Logic And Computer Design Solution Manual Budget-Friendly Options
6. Navigating Digital Logic And Computer Design Solution Manual eBook Formats

- ePub, PDF, MOBI, and More
- Digital Logic And Computer Design Solution Manual Compatibility with Devices
- Digital Logic And Computer Design Solution Manual Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Digital Logic And Computer Design Solution Manual
 - Highlighting and Note-Taking Digital Logic And Computer Design Solution Manual
 - Interactive Elements Digital Logic And Computer Design Solution Manual
- 8. Staying Engaged with Digital Logic And Computer Design Solution Manual
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Digital Logic And Computer Design Solution Manual
- 9. Balancing eBooks and Physical Books Digital Logic And Computer Design Solution Manual
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Digital Logic And Computer Design Solution Manual
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Digital Logic And Computer Design Solution Manual
 - Setting Reading Goals Digital Logic And Computer Design Solution Manual
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Digital Logic And Computer Design Solution Manual
 - Fact-Checking eBook Content of Digital Logic And Computer Design Solution Manual
 - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
- 14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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