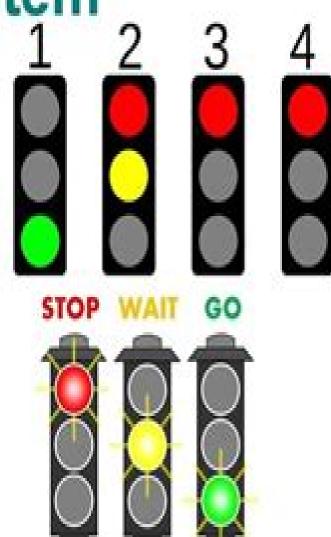
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Passau The work presented involves advanced specification languages for hardware design that are intuitive to the designer like timing diagrams and state based languages as well as their relation to VHDL and formal languages like temporal logic and a process algebraic calculus The results of experimental tests of the tools are also presented *VHDL for Logic Synthesis* Andrew Rushton,1995 This is the first book to detail the use of VHDL with logic synthesis techniques showing how to use the hardware description language to achieve SLSI design results It explains VHDL features in terms of the hardware mappings performed in synthesis basics then builds to more advanced topics like the writing of VHDL packages and the writing of effective text benches **Euro-DAC '95, European Design Automation Conference with Euro-VHDL**, 1995

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