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6.1 Does the inverter with a lower V_{OL} always have the shorter high-to-low switching time?

Justify your answer.

SOLUTION:

A low V_{OL} means that the transconductance k of the driver is higher than that of the load. This means that W/L of the driver must be relatively large, necessitating that it takes up more area. Thus, its capacitance will be higher on the average. So the high-to-low switching delay time might in fact be larger since $\tau = C_L \Delta V / I$.

6.2 Consider switching delays for 10 fF in a 10-k Ω resistive-load inverter circuit, where

$$\mu_n C_{ox} = 98.3 \text{ } \mu\text{A/V}^2$$

$$(W/L)_p = 10$$

$$V_{T,n} = 0.53 \text{ V}$$

$$E_{c,n} L_n = 0.4 \text{ V}$$

- (a) Find τ_{PHL} (50% high-to-low transition delay) by using the average-current method. Assume that the input signal is an ideal rectangular pulse switching between 0 and 1.2 V with zero rise/fall times. You will have to calculate V_{OL} to solve this problem.
- (b) By using an appropriate differential equation and the proper initial voltage across the capacitor (when the input voltage is at V_{OH}) which is V_{OL} and not 0 V, calculate τ_{PLH} . Use the same input voltage as in part (a).

SOLUTION:

(a)

First find V_{OL} : the transistor operates in linear region when $V_{DS} = V_{OL}$, therefore,

Cmos Digital Integrated Circuits Manual

John D. Lenk



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applications Chapter 3 deals with modern logic circuitry and Chapter 4 with CMOS bilateral switches and data selectors The next six chapters progress through waveform generator circuitry clocked flip flop and counter circuits ICs special counter dividers data latches registers comparators and code converters Chapter 11 focuses on specialised types of IC such as multiplexers and decoders while the final chapter presents a miscellaneous collection of useful CMOC circuits

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