

Encounter Timing System

Unified timing analysis for faster design closure and signoff

Timing and signal integrity analysis can consume a significant portion of the overall silicon realization design cycle. Using Cadence® Encounter® Timing System with Encounter Digital Implementation System, design teams benefit from an advanced timing analysis infrastructure that tightly couples the design implementation environment with the timing signoff environment. This improves timing convergence throughout the design flow and greatly reduces the time to design closure. As a complete standalone solution, Encounter Timing System offers silicon-accurate timing signoff and signal integrity analysis that ensures operational chips after tapeout.

Encounter Timing System

Industry-endorsed and production-proven on both mainstream and advanced technology node designs, Encounter Timing System is a full-chip static timing analysis (STA) solution providing gate-level delay calculation, signoff-level timing and signal integrity (SI) analysis, statistical timing and leakage analysis, advanced on-chip variation analysis, and advanced node functionality required for double-patterning and waveform effects.

Designers have traditionally relied on one timing method for design implementation and a different timing method for signoff analysis. This leads to over-design with excessive timing margins and additional iterations in order to meet timing convergence throughout the place-and-route flow and correlation to timing signoff analysis at the end of the design flow.

Encounter Timing System removes the iteration bottleneck by providing a consistent, integrated Common Timing Engine for both the design implementation stage and the final timing verification stage of the design cycle. The result is correlation and convergence between implementation and signoff for faster timing closure.



Figure 1: Unified timing for implementation and signoff provides faster design convergence and timing closure

Benefits

- Advanced timing solution with comprehensive analysis
 - Delay calculation
 - Static timing analysis
 - SI analysis
 - Statistical timing analysis
 - On-chip variation analysis
- Integrated with EDI System
 - Consistent timing analysis during implementation throughout the flow and signoff at the end of the flow
- Faster design convergence and timing closure with smaller design margin
- Common database infrastructure for fast setup and a consistent usage model throughout the flow
- Unmatched timing signoff accuracy
 - Prevents excessive over-design to exceed performance, power, and area targets
 - Delivers accurate base delay and SI delay calculation to within 2-5% of SPICE

Cadence Encounter Timing System User Manual

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Catthoor, Praveen Raghavan, Frederik
Naessens**



Cadence Encounter Timing System User Manual:

Energy-Efficient Communication Processors Robert Fasthuber, Francky Catthoor, Praveen Raghavan, Frederik Naessens, 2013-05-29 This book describes a new design approach for energy efficient Domain Specific Instruction set Processor DSIP architectures for the wireless baseband domain The innovative techniques presented enable co design of algorithms architectures and technology for efficient implementation of the most advanced technologies To demonstrate the feasibility of the author s design approach case studies are included for crucial functionality of advanced wireless systems with increased computational performance flexibility and reusability Designers using this approach will benefit from reduced development product costs and greater scalability to future process technology nodes *Circuits and Systems Advances in Near Threshold Computing* Sanghamitra Roy, 2021-05-11 Modern society is witnessing a sea change in ubiquitous computing in which people have embraced computing systems as an indispensable part of day to day existence Computation storage and communication abilities of smartphones for example have undergone monumental changes over the past decade However global emphasis on creating and sustaining green environments is leading to a rapid and ongoing proliferation of edge computing systems and applications As a broad spectrum of healthcare home and transport applications shift to the edge of the network near threshold computing NTC is emerging as one of the promising low power computing platforms An NTC device sets its supply voltage close to its threshold voltage dramatically reducing the energy consumption Despite showing substantial promise in terms of energy efficiency NTC is yet to see widescale commercial adoption This is because circuits and systems operating with NTC suffer from several problems including increased sensitivity to process variation reliability problems performance degradation and security vulnerabilities to name a few To realize its potential we need designs techniques and solutions to overcome these challenges associated with NTC circuits and systems The readers of this book will be able to familiarize themselves with recent advances in electronics systems focusing on near threshold computing

The VLSI Handbook Wai-Kai Chen, 2018-10-03 For the new millenium Wai Kai Chen introduced a monumental reference for the design analysis and prediction of VLSI circuits The VLSI Handbook Still a valuable tool for dealing with the most dynamic field in engineering this second edition includes 13 sections comprising nearly 100 chapters focused on the key concepts models and equations Written by a stellar international panel of expert contributors this handbook is a reliable comprehensive resource for real answers to practical problems It emphasizes fundamental theory underlying professional applications and also reflects key areas of industrial and research focus WHAT S IN THE SECOND EDITION Sections on Low power electronics and design VLSI signal processing Chapters on CMOS fabrication Content addressable memory Compound semiconductor RF circuits High speed circuit design principles SiGe HBT technology Bipolar junction transistor amplifiers Performance modeling and analysis using SystemC Design languages expanded from two chapters to twelve Testing of digital systems Structured for convenient navigation and loaded with practical solutions The VLSI Handbook Second Edition

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Proceedings of SLIP '07 ,2007 *Voice & Data* ,2005 **Electronic Business** ,2004 The management magazine for the electronics industry *The Art of Timing Closure* Khosrow Golshan,2021-08-05 The Art of Timing Closure is written using a hands on approach to describe advanced concepts and techniques using Multi Mode Multi Corner MMMC for an advanced ASIC design implementation It focuses on the physical design Static Timing Analysis STA formal and physical verification The scripts in this book are based on Cadence Encounter System™ However if the reader uses a different EDA tool that tool s commands are similar to those shown in this book The topics covered are as follows Data Structures Multi Mode Multi Corner Analysis Design Constraints Floorplan and Timing Placement and Timing Clock Tree Synthesis Final Route and Timing Design Signoff Rather than go into great technical depth the author emphasizes short clear descriptions which are implemented by references to authoritative manuscripts It is the goal of this book to capture the essence of physical design and timing analysis at each stage of the physical design and to show the reader that physical design and timing analysis engineering should be viewed as a single area of expertise This book is intended for anyone who is involved in ASIC design implementation starting from physical design to final design signoff Target audiences for this book are practicing ASIC design implementation engineers and students undertaking advanced courses in ASIC design

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Table of Contents Cadence Encounter Timing System User Manual

1. Understanding the eBook Cadence Encounter Timing System User Manual
 - The Rise of Digital Reading Cadence Encounter Timing System User Manual
 - Advantages of eBooks Over Traditional Books
2. Identifying Cadence Encounter Timing System User Manual
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Cadence Encounter Timing System User Manual
 - User-Friendly Interface
4. Exploring eBook Recommendations from Cadence Encounter Timing System User Manual
 - Personalized Recommendations
 - Cadence Encounter Timing System User Manual User Reviews and Ratings
 - Cadence Encounter Timing System User Manual and Bestseller Lists
5. Accessing Cadence Encounter Timing System User Manual Free and Paid eBooks
 - Cadence Encounter Timing System User Manual Public Domain eBooks
 - Cadence Encounter Timing System User Manual eBook Subscription Services
 - Cadence Encounter Timing System User Manual Budget-Friendly Options
6. Navigating Cadence Encounter Timing System User Manual eBook Formats

- ePub, PDF, MOBI, and More
- Cadence Encounter Timing System User Manual Compatibility with Devices
- Cadence Encounter Timing System User Manual Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Cadence Encounter Timing System User Manual
 - Highlighting and Note-Taking Cadence Encounter Timing System User Manual
 - Interactive Elements Cadence Encounter Timing System User Manual
- 8. Staying Engaged with Cadence Encounter Timing System User Manual
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Cadence Encounter Timing System User Manual
- 9. Balancing eBooks and Physical Books Cadence Encounter Timing System User Manual
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Cadence Encounter Timing System User Manual
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Cadence Encounter Timing System User Manual
 - Setting Reading Goals Cadence Encounter Timing System User Manual
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Cadence Encounter Timing System User Manual
 - Fact-Checking eBook Content of Cadence Encounter Timing System User Manual
 - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
- 14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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