

Encounter Timing System

Unified timing analysis for faster design closure and signoff

Timing and signal integrity analysis can consume a significant portion of the overall silicon realization design cycle. Using Cadence® Encounter® Timing System with Encounter Digital Implementation System, design teams benefit from an advanced timing analysis infrastructure that tightly couples the design implementation environment with the timing signoff environment. This improves timing convergence throughout the design flow and greatly reduces the time to design closure. As a complete standalone solution, Encounter Timing System offers silicon-accurate timing signoff and signal integrity analysis that ensures operational chips after tapeout.

Encounter Timing System

Industry-endorsed and production-proven on both mainstream and advanced technology node designs, Encounter Timing System is a full-chip static timing analysis (STA) solution providing gate-level delay calculation, signoff-level timing and signal integrity (SI) analysis, statistical timing and leakage analysis, advanced on-chip variation analysis, and advanced node functionality required for double-patterning and waveform effects.

Designers have traditionally relied on one timing method for design implementation and a different timing method for signoff analysis. This leads to over-design with excessive timing margins and additional iterations in order to meet timing convergence throughout the place-and-route flow and correlation to timing signoff analysis at the end of the design flow.

Encounter Timing System removes the iteration bottleneck by providing a consistent, integrated Common Timing Engine for both the design implementation stage and the final timing verification stage of the design cycle. The result is correlation and convergence between implementation and signoff for faster timing closure.



Figure 1: Unified timing for implementation and signoff provides faster design convergence and timing closure

Benefits

- Advanced timing solution with comprehensive analysis
 - Delay calculation
 - Static timing analysis
 - SI analysis
 - Statistical timing analysis
 - On-chip variation analysis
- Integrated with EDI System
 - Consistent timing analysis during implementation throughout the flow and signoff at the end of the flow
- Faster design convergence and timing closure with smaller design margin
- Common database infrastructure for fast setup and a consistent usage model throughout the flow
- Unmatched timing signoff accuracy
 - Prevents excessive over-design to exceed performance, power, and area targets
 - Delivers accurate base delay and SI delay calculation to within 2-5% of SPICE

Cadence Encounter Timing User Manual

Yi-Tong Ma



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Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits Sandeep K. Goel, Krishnendu Chakrabarty, 2017-12-19 Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits ICs. However, the increased complexity and nanometer size features of modern ICs make them susceptible to manufacturing defects as well as performance and quality issues. Testing for Small Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations, power supply noise, crosstalk, resistive opens, bridges, and design for manufacturing DfM related rule violations. The book also addresses testing for small delay defects SDDs which can cause immediate timing failures on both critical and non-critical paths in the circuit. Overviews semiconductor industry test challenges and the need for SDD testing including basic concepts and introductory material. Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics. Reviews SDD testing based on alternative methods that explore new metrics, top-off ATPG and circuit topology based solutions. Highlights the advantages and disadvantages of a diverse set of metrics and identifies scope for improvement. Written from the triple viewpoint of university researchers, EDA tool developers, and chip designers and tool users, this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective. The book is designed as a one-stop reference for current industrial practices, research challenges in the domain of SDD testing, and recent developments in SDD solutions. **Test and Diagnosis for Small-Delay Defects** Mohammad Tehranipoor, Ke Peng, Krishnendu Chakrabarty, 2011-09-08 This book will introduce new techniques for detecting and diagnosing small delay defects in integrated circuits. Although this sort of timing defect is commonly found in integrated circuits manufactured with nanometer technology, this will be the first book to introduce effective and scalable methodologies for screening and diagnosing small delay defects including important parameters such as process variations, crosstalk, and power supply noise. Circuits and Systems Advances in Near Threshold Computing Sanghamitra Roy, 2021-05-11 Modern society is witnessing a sea change in ubiquitous computing in which people have embraced computing systems as an indispensable part of day-to-day existence. Computation, storage, and communication abilities of smartphones, for example, have undergone monumental changes over the past decade. However, global emphasis on creating and sustaining green environments is leading to a rapid and ongoing proliferation of edge computing systems and applications. As a broad spectrum of healthcare, home, and transport applications shift to the edge of the network, near threshold computing (NTC) is emerging as one of the promising low-power computing platforms. An NTC device sets its supply voltage close to its threshold voltage, dramatically reducing the energy consumption. Despite showing substantial promise in terms of energy efficiency, NTC is yet to see widescale commercial adoption. This is because circuits and systems operating with NTC suffer from several problems, including increased sensitivity to process variation, reliability problems, performance degradation, and security vulnerabilities, to name a few. To realize its potential, we need designs

techniques and solutions to overcome these challenges associated with NTC circuits and systems The readers of this book will be able to familiarize themselves with recent advances in electronics systems focusing on near threshold computing

Energy-Efficient Communication Processors Robert Fasthuber, Francky Catthoor, Praveen Raghavan, Frederik Naessens, 2013-05-29 This book describes a new design approach for energy efficient Domain Specific Instruction set Processor DSIP architectures for the wireless baseband domain The innovative techniques presented enable co design of algorithms architectures and technology for efficient implementation of the most advanced technologies To demonstrate the feasibility of the author s design approach case studies are included for crucial functionality of advanced wireless systems with increased computational performance flexibility and reusability Designers using this approach will benefit from reduced development product costs and greater scalability to future process technology nodes

Nanometer Technology Designs Nisar Ahmed, 2010-02-26 Adopting new fabrication technologies not only provides higher integration and enhances performance but also increases the types of manufacturing defects With design size in millions of gates and working frequency in GHz timing related defects havv become a high proportion of the total chip defects For nanometer technology designs the stuck at fault test alone cannot ensure a high quality level of chips At speed tests using the transition fault model has become a requirement in technologies below 180nm Traditional at speed test methods cannot guarantee high quality test results as they face many new challenges Supply noise including IR drop ground bounce and Ldi dt effects on chip performance high test pattern volume low fault defect coverage small delay defect test pattern generation high cost of test implementation and application and utilizing low cost testers are among these challenges This book discusses these challenges in detail and proposes new techniques and methodologies to improve the overall quality of the transition fault test

Design and Process Integration for Microelectronic Manufacturing ,2005 FPGA ... ,2006 EDN ,2008
Synthesis Methodology for Built-in At-speed Testing Yinghua Li, 2005 *Voice & Data* ,2005 **Proceedings** ,2003
Infantry Journal ,1924 **Automotive Engineering ...** ,1916 **A Low Power Design Methodology with**
Multi-VDD and Voltage Islands Huaizhi Wu, 2007 **The Military Engineer** ,1923 Directory of members constitution and by laws of the Society of American military engineers 1935 inserted in v 27 **ASIC & EDA** ,1993 *Children's Faces Looking Up* Dorothy De Wit, 1979 Includes six sample programs and shows how the programs employ balance rhythm pacing and variety Electronic Business ,2004 The management magazine for the electronics industry **The United States Army and Navy Journal and Gazette of the Regular and Volunteer Forces** ,1885 **Dataquest** ,2007

Cadence Encounter Timing User Manual Book Review: Unveiling the Magic of Language

In an electronic digital era where connections and knowledge reign supreme, the enchanting power of language has become more apparent than ever. Its power to stir emotions, provoke thought, and instigate transformation is actually remarkable. This extraordinary book, aptly titled "**Cadence Encounter Timing User Manual**," published by a very acclaimed author, immerses readers in a captivating exploration of the significance of language and its profound effect on our existence. Throughout this critique, we will delve into the book's central themes, evaluate its unique writing style, and assess its overall influence on its readership.

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