University Syllabus
DSP Algorithms and Architecture

Subject Code	: **10EC751**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

PART - A

UNIT - 1

INTRODUCTION TO DIGITAL SIGNAL PROCESSING: Introduction, A Digital Signal-Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation. **5 Hours**

UNIT - 2

ARCHITECTURES FOR PROGRAMMABLE DIGITAL SIGNAL-PROCESSORS: Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Features for External Interfacing. **8 Hours**

UNIT - 3

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Introduction, Commercial digital Signal-processing Devices, Data Addressing Modes of TMS320C54xx., Memory Space of TMS320C54xx Processors, Program Control. **6 Hours**

UNIT - 4

Detail Study of TMS320C54X & 54xx Instructions and Programming, On-Chip peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54xx Processor. **6 Hours**

PART - B

UNIT - 5

IMPLEMENTATION OF BASIC DSP ALGORITHMS: Introduction, The Q-notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case). **6 Hours**

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